ABSTRACT

A device having at least one processor connected a controller and a memory; where the controller to execute a debug process. The debug process attaches a breakpoint bit field to each instruction. A system having image signal processors (ISPs), each ISP including processor elements (PEs). The ISPs include a debug instruction register connected to a first mux element. An instruction memory is connected to an instruction register. A decoder is connected to the instruction register. An execution unit is connected to the decoder. A debug executive unit is connected to the instruction memory, and a second mux element is connected to the execution unit and local registers. The decoder decodes a breakpoint bit field of each instruction.